WHAT IS CLAIMED IS:

1. An ESD protection circuit, comprising:

one or more first diodes coupled in series between a supply voltage and a terminal pad;

a second diode coupled to a ground; and

one or more third diodes coupled in series between said terminal pad and said second diode, wherein said one or more third diodes are configured to enable a voltage on an interconnection node between said one or more third diodes and said second diode that is different from ground;

wherein said ESD protection circuit increases the allowable signal swing at said terminal pad.

2. The ESD protection circuit of claim 1, wherein said one or more third diodes include an n+ on an area of P-substrate surrounded by a deep N-well.

3. The ESD protection circuit of claim 2, wherein said deep N-well separates said area of P-substrate from a common area of P-substrate.

4. The ESD protection circuit of claim 3, wherein said common area of P-substrate is coupled to said ground.

5. The ESD protection circuit of claim 1, wherein said allowable signal swing at said terminal pad is greater than said supply voltage plus 1.4 V.

6. The ESD protection circuit of claim 1, wherein a forward turn-on voltage of said one or more first diodes, said second diode, and said one or more third diodes is approximately 0.7 V.

7. An ESD protection circuit, comprising:

one or more of a first diode coupled in series between a supply voltage and a terminal pad;

a second diode coupled to a ground; and

one or more of a third diode coupled in series between said terminal pad and said second diode, wherein said one or more third diodes includes an n+ on an area of P-substrate separated by a deep N-well from a common area of P-substrate;

wherein said ESD protection circuit increases the allowable signal swing at said terminal pad.

8. The ESD protection circuit of claim 7, wherein said one or more first diodes include a p+ in an N-well on said common area of P-substrate.

9. The ESD protection circuit of claim 7, wherein said second diode includes an n+ on said common area of P-substrate.

10. The ESD protection circuit of claim 7, wherein said common area of P-substrate is coupled to said ground.

11. The ESD protection circuit of claim 7, wherein said allowable signal swing at said terminal pad is greater than said supply voltage plus 1.4 V.

12. The ESD protection circuit of claim 7, wherein a forward turn-on voltage of said one or more first diodes, said second diode, and said one or more third diodes is approximately 0.7 V.

13. An ESD protection circuit, comprising:

a first diode having a cathode coupled to a supply voltage and an anode coupled to a cathode of a second diode, said second diode having an anode coupled to a terminal pad; and

a third diode having a cathode coupled to said terminal pad and an anode coupled to a cathode of a fourth diode, said fourth diode having an anode coupled to a ground, wherein said third diode includes an n+ on an area of P-substrate separated by a deep N-well from a common area of P-substrate;

wherein said ESD protection circuit increases the allowable signal swing at said terminal pad.

14. The ESD protection circuit of claim 13, wherein said first diode and said second diode include an n+ in an N-well on said common area of P-substrate.

15. The ESD protection circuit of claim 13, wherein said fourth diode includes an n+ on said common area of P-substrate.

16. The ESD protection circuit of claim 13, wherein said common area of P-substrate is coupled to said ground.

17. The ESD protection circuit of claim 13, wherein said allowable signal swing at said terminal pad is greater than said supply voltage plus 1.4 V.

18. The ESD protection circuit of claim 13, wherein a forward turn-on voltage of said first diode, said second diode, said third diode, and said fourth diode is approximately 0.7 V.